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US Patent Nr.	Title	Assignee	Filed	Date of Patent
6512273	Method and structure for improving hot carrier immunity for devices with very shallow junctions	AMD	1/28/00	1/28/03
6511911	Metal gate stack with etch stop layer	AMD	4/3/01	1/28/03
6512266	Method of fabricating SiO2 spacers and annealing caps	IBM	7/11/01	1/28/03
6512269	High-voltage high-speed SOI MOSFET	IBM	9/7/00	1/28/03
6514378	Method for improving uniformity and reducing etch rate variation of etching polysilicon	LAM	3/31/00	2/4/03
6514390	Method to eliminate coil sputtering in an ICP source	AMAT	10/17/96	2/4/03
6514843	Method of enhanced oxidation of MOS transistor gate corners	IBM	4/27/01	2/4/03
6514871	Gate etch process with extended CD trim capability	AMD	6/19/00	2/4/03
6518190	Plasma reactor with dry clean apparatus and method	AMAT	12/23/99	2/11/03