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Color Code:

Red – Plasma Etching

Blue – Advanced Devices

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<http://patft.uspto.gov/netahtml/srchnum.htm>

US Patent Nr.	Title	Assignee	Filed	Date of Patent
6,599,813	Method of forming shallow trench isolation for thin silicon-on-insulator substrates	International Business Machines Corporation	6/29/01	7/29/03
6,586,314	Method of forming shallow trench isolation regions with improved corner rounding	Chartered Semiconductor Manufacturing Ltd.	10/8/02	7/1/03
6,589,709	Process for preventing deformation of patterned photoresist features	Advanced Micro Devices	3/28/01	7/8/03
6,589,869	Film thickness control using spectral interferometry	Applied Materials Inc.	4/23/02	7/8/03
6,589,879	Nitride open etch process based on trifluoromethane and sulfur hexafluoride	Applied Materials Inc.	1/18/01	7/8/03
6,589,884	Method of forming an inset in a tungsten silicide layer in a transistor gate stack	Micron Technology, Inc.	8/31/00	7/8/03
6,590,231	Transistor that uses carbon nanotube ring	Fuji Xerox Co.	8/8/01	7/8/03

6,593,187	Method to fabricate a square poly spacer in flash	Taiwan Semiconductor Manufacturing Co.	8/27/01	7/15/03
6,593,197	Sidewall spacer based fet alignment technology	Advanced Micro Devices	3/19/01	7/15/03
6,593,232	Plasma etch method with enhanced endpoint detection	Taiwan Semiconductor Manufacturing Co.	7/5/02	7/15/03
6,593,241	Method of planarizing a semiconductor device using a high density plasma system	Applied Materials Inc.	5/11/98	7/15/03
6,593,244	Process for etching conductors at high etch rates	Applied Materials Inc.	9/11/00	7/15/03
6,593,245	Silicon nitride etch process with critical dimension gain	Advanced Micro Devices	8/1/96	7/15/03
6,593,617	Field effect transistors with vertical gate side walls and method for making such transistors	International Business Machines Corporation	2/19/98	7/15/03
6,596,554	Body-tied-to-source partially depleted SOI MOSFET	Texas Instruments Incorporated	11/27/01	7/22/03
6,596,605	Method of forming germanium doped polycrystalline silicon gate of MOS transistor and method of forming CMOS transistor device using the same	Samsung Electronics Co., Ltd.	12/28/00	7/22/03

6,596,609	Method of fabricating a feature in an integrated circuit using two edge definition layers and a spacer	Intel Corporation	12/19/00	7/22/03
6,597,203	CMOS gate array with vertical transistors	Micron Technology, Inc.	3/14/01	7/22/03
6,599,437	Method of etching organic antireflection coating (ARC) layers	Applied Materials Inc.	3/20/01	7/29/03
6,600,170	CMOS with strained silicon channel NMOS and silicon germanium channel PMOS	Advanced Micro Devices	12/17/01	7/29/03