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Etch Mechanisms

“Formation of Ammonium Salts and Their Effects on Controlling Pattern Geometry in the Reactive Ion Etching Process for Fabricating Aluminum Wiring and Polysilicon Gate”

S. Saito, K. Sugita, J. Tonotani, M. Yamage
Jpn. J. Appl. Phys. Vol. 41 (2002) pp. 2220 - 2224

This paper studies the effect of nitrogen addition to chlorine based Al and HBr / Cl₂ based poly-Si chemistries. In both cases, the addition of nitrogen leads to more tapered (or less notched) profiles. While this effect is well known and used in industrial scale production, the passivation mechanism for nitrogen addition is not understood. In the case of poly-Si etching, the formation of silicon nitride reaction products on the feature sidewalls had been proposed previously. Saito and coworkers use FT-IR, AES, XPS and TDS surface analysis methods to show that the ammonium salts such as NH₄AlCl₄ in the case of Al etching and (NH₄)₂SiBr₆ in the case of poly-Si etching are formed on the feature sidewalls. The source of hydrogen is the resist in the case of Al etching and HBr in the case of hardmask WSix/Si stack etching.

Modeling of Plasma Etching

“Multiscale Modeling of Plasma Etch Processing”

V. Sukharev
Vacuum Vol. 65 (2002) pp. 281 - 289

This paper gives a very good overview of the status of multi-scale modeling of plasma assisted semiconductor processing. Commercial reactor, sheath and feature scale models are presented. The author points out that the proper link between the simulation models has not yet been deployed. Feature scale feedback is an outstanding issue.

Plasma Diagnostics

“Diagnostics of a Wafer Interface of a Pulsed Two-Frequency Capacitively Coupled Plasma for Oxide Etching by Emission Selected Computerized Tomography”

T. Fujita, T. Makabe
Plasma Sources Sci. Technol. Vol. 11 (2002) pp. 142 – 145

This paper reports results of Computerized Tomography (CT) measurements of an interface close to a SiO₂ wafer being etched in a 2f-CCP system. CF₄/Ar and Ar plasmas at 25 mTorr are sustained with 100 MHz VHF source power which is pulsed. The bias power has a frequency of 500 kHz. The experimental results predict that the double layered sheath structure is interacting with the wafer biased with a low frequency RF field. Negatively charged particles can be accelerated to the wafer surface from the CF₄/Ar plasma under these conditions. Feature sidewall neutralization by negatively charged ions is a desired effect in high aspect ratio dielectric etching.

“Measurements and Modelling of Ion Energy Distributions in High-Density, Radio-Frequency Biased CF₄ Discharges”

M.A. Sobolewski, Y. Wang, A. Goyette
J. Appl. Phys. Vol. 91 (2002) pp. 6303 – 6314

Ion energy distributions (IED's) for 10 mTorr high density ICP CF₄ plasmas have been measured. The ion energies were measured with a grounded energy analyzer / mass spectrometer, i.e. the

IED's were measured for the grounded walls, not the biased cathode. Biasing effects could be measured due to the additional voltage developed across the ground sheath when bias power is applied. The measurements show good agreement with a sheath model described previously. Input parameters (time averaged current density and plasma potential) were measured with the experimental setup. The electron temperature was taken from the literature. The model was found to predict IED's well for the entire range of bias frequencies, even for intermediate frequencies when the ion transit time is comparable to the RF bias period.

Devices

"Impact of Floating Gate Dry Etching on Erase Characteristics in NOR Flash Memory"

W.H. Lee, D.K. Lee, Y.H. Na, K.S. Kim, K.O. Ahn, K.D. Suh, Y.H. Roh
IEEE Electron Devices Letters, Vol. 23 (2002) pp. 476 – 478

The impact of plasma damage effects on erase characteristics of flash memory cells has been investigated. The effect of fast erasing bits could be traced back to plasma damage effects in a non optimized plasma during the floating gate etch process. The experimental results indicate that the physical effect responsible for the fast erasing bits are clusters of positive charges near the poly-Si / SiO₂ interface.

"The Vertical Replacement-Gate (VRG) MOSFET"

J.M. Hergenrother, S.H. Oh, D. Monroe, F.P. Klemens, A. Kornblit
Solid-State Electronics Vol. 46 (2002) 939 – 950

A very detailed description of the formation and integration of vertical replacement gate (VRG) MOSFET's. The VRG-MOSFET is aimed at memory as well as at high performance and high speed logic. High performance devices with 50 nm physical gate length have been demonstrated without advanced lithography. The key features of this device are a gate oxide that is grown on single crystal silicon, self-aligned source/drain extensions formed by solid source diffusion, small parasitic overlap, junction, and source/drain capacitances, as well as a replacement gate approach that enables alternative stacks.

"FinFET Design Considerations Based on 3-D Simulation and Analytical Modeling"

G. Pei, J. Kedzierski, P. Oldiges, M. Jeong, E.C. Kan
IEEE Transactions on Electron Devices Vol. 49 (2002) pp. 1411 – 1419

3D simulations of FinFET devices are presented. The model predicts a bump in the drain voltage vs. gate current curve that is caused by corner effects of the silicon sliver that represents the Fin. The elimination of these corners could be a technological challenge.