

Literature Digest
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Special Edition: The Highlights of the IEDM 2002

FinFETs

25 nm CMOS Omega FETs

F.L.Yang et al.

A new transistor structure, called Omega FET, is introduced by TSMC. The gate wraps almost around the entire silicon channel, except for the part bottom surface of the device, which is resting on a rim etched into the buried oxide. The extension of the gate underneath the device and the top gate allow the use of a thicker silicon body. The latter can be higher than for a FD-SOI device (or Ultra-thin-body FET, or depleted substrate transistor DST) and wider than for a FinFET. An optimal Ω -FET will have a silicon body (channel) with a height larger or equal two times the gate length and a width equal to the gate length. Because of the wider body, the Ω -FET has a **reduced body thickness sensitivity**, a reduced parasitic resistance, does not need raised source/drains and does not require patterning of features smaller than the gate length.

Two version of the device are presented in the paper: a 1V version for low leakage, and a 0.7 V version for low active power. For the latter, gate delays (CV/I) of 0.39 ps for n-FET and 0.88 ps for p-FET are reported. These values are only around 30 % of the values given in the 2001 ITRS roadmap 2001 for devices with a gate length of 25 nm.

For device performance comparison see: http://www.clarycon.com/transistor_perfo.html

FinFET Scaling to 10 nm Gate Length

Bin Yu et al.

This joint paper by AMD and UC Berkley reports the smallest double gate transistors ever fabricated with a gate length of 10 nm and a Fin width of 12 nm. The vertical sidewalls of the silicon Fin are **oriented in <110>** direction, which leads to very good hole mobilities for the PMOS device. The Si Fin and the gate were patterned with 193 nm and 248 nm wavelength optical lithography, respectively. A not specified pattern reduction technique was used to get down to the aforementioned dimensions. Gate delays (CV/I) of 0.34 ps for the n-FET and 0.43 ps for the p-FET were achieved.

For device performance comparison see: http://www.clarycon.com/transistor_perfo.html

Metal Gates

Metal-gate FinFET and fully-depleted SOI devices using total gate silicidation

J. Kedzierski et al.

A broad range of thin body devices is covered in this paper by IBM: FinFET's with metal silicide gates and undoped body, FinFET's with poly-Si gates and doped body, FD-SOI devices with metal silicide gates and undoped body. Six different metal silicides were studied: **CoSi₂, CoSi, NiSi₂, NiSi, PdSi, and Co_{(1-x)Ni_(x)Si₂}**. Two methods to achieve the proper workfunction for the metal silicide FinFET's and FD SOI are studied: silicon substitutional doping with arsenic, boron and phosphorous and metal substitution (adjustment of the Co to Ni ratio in Co_{(1-x)Ni_(x)Si₂}).

The Fin FET's were fabricated with **selective SI epi raised source/drain** (CoSi₂ RSD). CMP was used to separate the RSD and gate silicidations. The FinFET's had a T_{ox} of 1.6 nm, and Fin thickness of 25 nm, high tilt extension implants, and an <110> crystal orientation of the Fin. The gate length was larger than 100 nm. Neither body, well, or halo implants were used in the FD SOI devices, V_t was controlled solely through silicide Φ_m engineering.

For device performance comparison see: http://www.clarycon.com/transistor_perfo.html

75 nm Damascene Metal Gate and High-k integration for Advanced CMOS Devices

B. Guillaumont et al.

STM presents a 75 nm damascene gate device with HfO₂ (EOT's from 1.35 to 2.27 nm) and CVD TiN and W gates for workfunction control. The I_{off} was only 1 pA for the n-MOSFET and 10 pA for the p-MOSFET at V_d=0.9V.

Transistors with Dual Work Function Metal Gates by Single Full Silicidation (FUSI) of Polysilicon Gates

W.P. Maszara et al.

AMD presents dual work function metal gate SOI transistors with **NiSi gates** and source drains. The work functions were ~4.5 eV for the NMOS and ~4.9 eV for the PMOS. The shift in Φ_m is explained by As accumulation at the gate/dielectric interface as a result of As segregation on front of the advancing silicide front during the silicidation process. This is confirmed with AES measurements which show 60 atomic % As at the interface, which is 50 % of the entire implanted dose.

Nickel Silicide Metal Gate FDSOI Devices with Improved Gate Oxide Leakage

Z. Krivokapic et al.

AMD presents a nickel silicide gate FDSOI device with undoped channel, 2 nm Gox, and symmetric V_t for NMOS and PMOS devices. The EOT is 0.6 nm thinner compared to a poly-Si gate because of the elimination of poly-Si depletion. The **gate oxide** was found to be a **good barrier for nickel**. Nickel silicide has the advantage of a low silicidation temperature.

High k Dielectrics

Nitrogen Concentration Effects and Performance Improvement of MOSFETs Using Thermally Stable HfO_xN_y Gate Dielectrics

Chang Seok Kang et al.

This paper by the Microelectronics Research Center of the University of Texas Austin studies the effects of nitrogen concentration on the material and electrical properties of HfO_xN_y gate dielectrics. A reduction in boron penetration and hence a smaller shift in flatband voltage is reported when the nitrogen concentration of the film is increased. On the other hand, the mobility is severely degraded for higher nitrogen concentrations. This is in contrast to the behavior of HfSiO, which shows an improvement in mobility when nitrogen is incorporated (A.L.P. Rotondaro et al., 2002 Symp. VLSI Tech. Papers, p. 148).

Effects of Nitrogen in HfSiON Gate Dielectrics on the Electrical and Thermal Characteristics

M. Koyama et al.

This research team from Toshiba provides additional evidence that nitrogen enhances the dielectric constant of hafnium silicate. High dielectric constants of the HfSiON are maintained and

boron penetration is substantially suppressed in the HfSiON during high temperature annealing. Higher k values were found for higher Hf and N concentrations. The highest value of $k=13$ was obtained for $Hf/Hf+Si=0.4$ and $N/Hf+Si+O+N=0.23$. While nearly ideal V_{fb} values were obtained for n^+ devices, V_{fb} is shifted significantly for p^+ devices. It is speculated that this is the result of the formation of positively charged defects by the interaction between Hf and B. The authors state that HfSiON is the most likely candidate for the first generation high k materials.

Planar Ultra Thin Body Devices

Extreme Scaling with Ultra-Thin Si Channel MOSFET's

B. Doris et al.

This paper by an IBM research team presents characteristics of extremely scaled devices with physical gate lengths down to 6 nm and SOI channels as thin as 4 nm. The SOI films were thinned by thermal oxidation and wet etching. The sub-lithographic dimensions were achieved with aggressive trimming. The **gate stack and nitride spacer etch** were developed specifically to **minimize Si consumption** in the source and drain regions. Raised source/drains were used to reduce the parasitic resistance. The 6 nm device could be turned off, but the saturation current was only $130 \mu A/\mu m$ at $V_{dd}=1.5$ V due to process induced variations such as high halo implant concentration and increased series resistance under the spacer.

For device performance comparison see: http://www.clarycon.com/transistor_perfo.html

SON (Silicon-On-Nothing) P-MOSFET's with totally silicided (CoSi₂) Polysilicon on 5 nm-thick Si-films: The simplest way to integration of Metal Gates on thin FD channels

S. Monfray et al.

STM presents the first SON device with metal gate. The SON devices were performed with 55 nm CoSi₂ gate length and 5 nm of Si-channel thickness. The very thin channel reduces the short channel effect (lower Drain Induced Barrier Lowering DIBL) but also reduces V_t , which would lead to intolerably high off currents. This can be countered by increasing the channel doping in the range of 6 to 8 E18 cm⁻³. This however degrades the mobility in the channel. **Mid-gap gates are required for V_t adjustment without mobility loss** at lowly doped channels. They also offer advantages by reducing poly depletion in the gate and gate resistance reduction. SON MOSFET's are uniquely suited for total gate silicidation because the Co reacts with the mono-Si of the bulk without lateral extend into the channel. The presented p-MOSFET device shows excellent SCE immunity with only 60 mV of DIBL and a subthreshold slope of 73 mV/dec. The I_{on} is $350 \mu A/\mu m$ and I_{off} is very low with 0.1 nA at $V_{dd}=1.4$ V.

For device performance comparison see: http://www.clarycon.com/transistor_perfo.html

Strained Silicon

Sub-30 nm P⁺ abrupt junction formation in Strained Si/Si_{1-x}Ge_x MOS device

K.L. Lee et al.

The research team from IBM reports that **shallower boron junctions can be achieved in strained Si/Si_{1-x}Ge_x than in bulk Si**. This trend improves with a thinner silicon cap (strained layer) and higher Ge concentration in the relaxed buffer layer. This adds another benefit to the strained silicon technique besides enhanced hole mobility and better boron activation.

Performance enhancement on sub-70 nm strained silicon SOI MOSFET's on Ultra-thin Thermally Mixed Strained Si/Ge on Insulator (TM-SGOI) substrate with Raised S/D

B.H. Lee et al.

IBM presents an ultra-thin TM-SGOI device with $T_{\text{SOI}} < 55$ nm that combines the benefits of strained silicon and SOI. 80 to 90 % $I_{\text{d,sat}}$ and mobility improvements are shown in long channel nFET devices. 20 to 25 % performance enhancement is demonstrated in short channel nFET devices.

Scaling of Bulk Devices

14 nm Gate Length CMOSFET's Utilizing Low Thermal Budget Process with Poly-SiGe and Ni Salicide

A. Hokazono et al.

In this paper by Toshiba, high performance 14 nm gate length CMOSFET's are presented. The focus was on the optimization of the offset spacer width and implantation condition for the extension region to improve the short channel effect and dose loss. A **poly-SiGe electrode and nickel salicidation** were chosen to enable the use of low temperature spike annealing. The gate oxide was a SiO_2 film, which was treated with a nitrogen plasma. For a V_{dd} of 0.8 V, a drive current of $640 \mu\text{A}/\mu\text{m}$ for the nMOS and $306 \mu\text{A}/\mu\text{m}$ for the pMOS were achieved. This are record values for 14 nm MOSFET's.

For device performance comparison see: http://www.clarycon.com/transistor_perfo.html

Raised Source Drain

High Performance Damascene Gate CMOSFET's with Recessed Channel Formed by Plasma Oxidation and Etching Method (RC-POEM)

K. Matsuo et al.

Toshiba reports on a device with a channel that is recessed into the substrate. This forms essentially **pseudo recessed source/drains** without the use of selective epitaxy. The recess is formed in an inlay gate scheme with ion assisted substrate oxidation and removal by wet etching. The method is shown to suppress short channel effects down to 35 nm gate length. High drive currents of $963 \mu\text{A}/\mu\text{m}$ for the nFET and $327 \mu\text{A}/\mu\text{m}$ have been achieved.

For device performance comparison see: http://www.clarycon.com/transistor_perfo.html

Line Edge Roughness

Line Edge Roughness: Characterization, Modeling and Impact on Device Behavior

J.A. Croon et al.

This IMEC report suggests that Line Edge Roughness (LER) **has no impact on 80 nm** gate length transistors. Simulations show that LER will become significant for 32 nm channel length devices. The analysis of experimental data shows high frequency line width fluctuations (< 1 nm) with a standard deviation σ_{HF} of 0.72 nm and low frequency contributions with a standard deviation σ_{LF} of 2.07 nm. The period of the low frequency is a characteristic width W_c . A new figure of merit is proposed for improving photolithography benchmarking: $W_c^{1/2} \sigma_{\text{LF}}$.

Determination of the Line Edge Roughness Specification for 34 nm Devices

T. Linton et al.

This paper is published by the Intel TCAD group. The authors conclude in agreement with the aforementioned IMEC paper that **LER is negligible for 130 nm technology**. They predict that **LER will play a significant role for 34 nm devices**. To study the LER effect, experimental splits were carried out on 70 nm devices in a 130 nm process technology. The different LER values were generated using different types of resists and exposure variations. The LER was deduced from top down SEM pictures and analyzed by a statistical method that uses a statistical ensemble of devices constructed from 2D slices. The results for $I_{d,sat}$ and I_{off} as a function of LER are in good agreement between the measured and calculated values. The statistical method was applied to 34 nm devices and a 3σ spec of 3 nm was derived.

Carbon Nano Tubes***Carbon Nanotube Electronics***

P. Avouris et al.

The IBM Yorktown team gives a brief review of the electronic properties of CNT's and presents results on the fabrication and characteristics of carbon nanotube field effect transistors (CNFETs) and simple integrated circuits. Air exposed CNFETs with thick gate oxides are p-type. N-type CNFETs can be made by simply annealing the p-type devices under vacuum to remove the adsorbed oxygen. This behavior is explained by the adsorption of oxygen at the metal electrode – nanotube junction. A technique is presented how to separate metallic CNTs and semiconducting CNTs. A current is passed through a bundle of CNTs which leads to the destruction of the m-CNTs, while the s-CNTs remain intact. The catalyst-free growth of oriented single-wall CNTs by thermal annealing of SiC to 1650°C under ultrahigh vacuum conditions is also shown.