

Literature Digest Vol. 4: January 2003

Modeling of Plasma Etching

“Effect of Neutral Transport on the Etch Product Lifecycle During Plasma Etching of Silicon in Chlorine Gas”

M.W. Kiehlbauch, D.B. Graves

J. Vac. Sci. Technol. A21 (2002) 116

The lifecycle of silicon containing etch products in silicon etching with a chlorine plasma has been modeled. A significant difference in the efficiency of etch product removal and chamber wall deposition for center and side gas injection as well as a showerhead configuration is reported. For the side injection and showerhead configurations, there is no significant convective flow at the wafer for any modeled flow rate. An increase of the total flow leads to a reduction of wall re-deposition due to a reduction in residence time. With the center inlet and a flow of 500 sccm, convective flow at the wafer is observed in the calculation. This drives the etch byproducts towards the gas outlet and reduces their concentration and chamber wall re-deposition. The effect of the gas injection geometry influences the amounts of ion and neutral redeposition and may have important consequences for the etch profiles and critical dimensions.

Etch Mechanisms: Chamber Wall Effects

“Influences of Reaction Products on Etch Rates and Linewidths in a Poly-Si/Oxide Etching Process Using HBr/O₂ Based Inductively Coupled Plasmas”

K. Miwa, T. Mukai

J. Vac. Sci. Technol. B 20 (2002) 2120

Variations of etch rates and line widths due to various seasoning methods after plasma cleaning of an etch chamber in a poly-Si/SiO₂ etch process are studied. The poly-Si etch rate for a low pressure process (3 mTorr main etch process) was found to be independent on the seasoning time. The oxide etch rate for the same process decreased and reached negative values (deposition) when the seasoning was done with silicon wafers (breakthrough / man etch). The results suggest that the etch rate of poly-Si and especially oxide are influenced by SiBr_x reaction products originating from the silicon oxyhalogenide covered chamber walls.

“Ion Flux Composition in HBr/Cl₂/O₂ and HBr/Cl₂/O₂/CF₄ Chemistries During Silicon Etching in Industrial High-Density Plasmas”

G. Cunge, R.L. Inglebert, O. Joubert, L. Vallier

J. Vac. Sci. Technol. B 20 (2002) 2137

Cunge et al. report on quantitative ion mass spectroscopy studies of widely used HBr/Cl₂/O₂ and HBr/Cl₂/CF₄/O₂ plasmas in an industrial silicon etch reactor. It is found, that SiCl_xBr_y⁺ ions represent more than 50% of the ion flux for the HBr/Cl₂/O₂ plasma. This is surprising since at the given pressure of 4 mTorr, a total gas flow of 200 scc and an etch rate of 2000 Å/min, the flow of silicon containing species from an 8 inch wafer should be only 6% of the halogen parent gas flow. The large concentration of silicon containing species is explained by a combination of the loading effect and lower ionization energy thresholds of halogenated silicon etch byproducts (Cl: 12.97 eV; Br: 11.81 eV; Si: 7.41 eV; SiBr: 7.3 eV; SiF: 7.28 eV; SiCl: 6.79 eV). **Bias power effect:** Increase of Si containing species with bias power following closely etch rate trend. **Source power effect at constant ion energy:** Ion flux of all species increase with Si containing species density

increasing slightly. Si^+ becomes dominant ion for powers above 1000 W. **Oxygen flow effect:** Etch rate goes through maximum but halogenated Si ion density decreases. Bromine and chlorine ion densities are increasing. This is explained by enhanced sticking of Si containing ions to the chamber wall in the presence of SiO_x on the chamber walls. **Effect of CF_4 addition:** Sum of halogenated silicon ionized species is reduced to less than 25 % for 13 % CF_4 addition to the total flow. Br and Cl represent 53 % of total flux. Among carbon containing species CF_3^+ has the highest concentration with 9 %. These changes in the ion mix affect the etch behavior deeply and not been considered adequately in feature evolution modeling studies.

“Effect of Surface Polymerization on Plasma and Process Stability in Polycrystalline-Silicon Etching”

S. Xu, Th. Lill, S. Deshmukh, O. Joubert
J. Vac. Sci. Technol. A 20 (2002) 2123

In this paper, free radical densities, etch rates and gate line widths for poly-Si gate etching in a Cl_2 , HBr, and O_2 containing plasma have been studied for different chamber wall conditions: anodized aluminum, silicon oxide, and fluorocarbon polymers. In general, the halogen radical concentration is higher in an oxide-coated chamber than in a clean chamber (anodized aluminum), while it is the lowest in a polymer coated chamber. The difference in Cl radical density between a clean and polymer coated chamber is very small. The fluorine content of the polymer coverage does not influence Cl or Br radical densities. Oxygen radical densities drop significantly in the presence of carbon on the chamber walls due to the consumption of oxygen in the carbon / oxygen reaction. These findings have implications for in-situ mask open processes where fluorocarbon polymers can be formed during the mask open process and silicon oxide based polymers during softlanding and overetch. In addition, CF_4 addition to the main etch can be a source of fluorocarbon polymers as well.

Etch Mechanisms: Beam Studies

“Argon and Oxygen Ion Chemistry Effects in Photoresist Etching”

F. Greer, L. Van, D. Fraser, J.W. Coburn, D.B. Graves
J. Vac. Sci. Technol. B 20 (2002) 1901

I-line resist etch rate kinetics have been studied in a beam apparatus using argon and oxygen ion beams together with a fluorine atom source. The etch yield of PR with oxygen was always higher than with argon, but the difference between the two gases decreased as the F atom/ion flux was increased. The increase of etch yield in the presence of oxygen ions is suggested to be the result of the formation of $\text{C}_x\text{F}_y\text{O}_z$ compounds. Energy and angular dependences of the resist removal rate for oxygen and argon ions are similar to those typically observed for physical sputtering.

Devices

“Advanced CMOS Transistors With a Novel HfSiON Gate Dielectric”

A.L.P. Rotondaro, M.R. Visokay, J.J. Chambers, A. Shanware, R. Khamankar, H. Bu, R.T. Laaksonen, L. Tsung, M. Douglas, R. Kuan, M.J. Bevan, T. Grinder, J. McPerson, L. Colombo / Texas Instruments
2002 Symposium On VLSI Technology, Digest of Technical Papers, p. 148

This paper reports on the fabrication of a short channel transistor using a **HfSiON** gate dielectric material. HfSiON has superior electrical characteristics such as low leakage current relative to SiO_2 , low interfacial trap density, electron and hole carrier mobilities ~ 80% of the universal curve at $E_{\text{eff}} > 0.8$ MV/cm and scalability to EOT of less than 10 Å. HfSiON is also thermally stable up to

1100 °C in contact with poly-Si, blocks boron significantly better than SiO₂ and SiON. CV curves indicate that the flat band voltage for the PMOS device is shifted potentially due to fixed charge in the dielectric.

“60 nm Gate Length Dual-V_t CMOS for High Performance Applications”

M. Mehrotra, J. Wu, A. Jain, T. Laaksonen, K. Kim, W. Bather, R. Koshy, J. Chen, J. Jacobs, V. Ukraintsev, L. Olsen, J. DeLoach, J. Mehigan, R. Agarwal, S. Walsh, D. Sekel, L. Tsung, M. Vaidyanathan, B. Trentman, K. Liu, S. Aur, R. Khamankar, P. Nicollian, Q. Jiang, Y. Xu, B. Campbell, P. Tiner, R. Wise, D. Scott, M. Rodder / Texas Instruments
2002 Symposium On VLSI Technology, Digest of Technical Papers, p. 124

A 60 nm CMOS for high performance applications at the 130 nm node is presented. The technology utilizes 193 nm lithography, dual spacers with thin spacer before drain extension implant and L-shaped nitride spacer after drain extension, and remote-plasma nitride dielectric with 1.75 nm EOT. The thin nitride spacer prior SDE implant minimizes series resistance while achieving low gate/drain overlap capacitance (C_{gd}). From a plasma etch point of view, the presented relationship between line edge roughness (**LER**) and drive current degradation is interesting. A typical LER of 30 to 35 Å results in a drive current loss of 3 % for NMOS and 5 % for PMOS.

For device performance comparison see: http://www.clarycon.com/transistor_perfo.html

“35 nm CMOS FinFETs”

F.L. Yang, H.Y. Chen, F.C. Chen, Y.L. Chan, K.N. Yang, C.J. Chen, H.J. Tao, Y.K. Choi, M.S. Liang, C. Hu / Taiwan Semiconductor Manufacturing Company
2002 Symposium On VLSI Technology, Digest of Technical Papers, p. 104

A high performance 35 nm CMOS **FinFET** is demonstrated. The double-gate FinFET structure does not require ultra shallow junctions to control short channel effects, the gate spacers can be shortened to reduce parasitic series resistance and raise drive currents, and the DIBL (Drain Induced Barrier Lowering) effect is reduced. **Process flow:** (100) SOI is thinned to 75 nm (Fin height). Fin patterning with oxide hardmask (9 nm after etch). Channel doping with masked ion implantation for NMOS and PMOS V_t adjustment. 24Å sacrificial thermal oxide removal before gate oxide growth. Deposition of heavily N⁺ doped poly-Si for gate formation. Plasma etch patterning and NFET source/drain extension implantation and anneal. Composite oxide/nitride spacer deposition and etch to final thickness of 30 nm. N⁺ and P⁺ junction formation by P and B implantation and activation at 1050 °C anneal. Cobalt silicide formation on source/drain and gate to minimize parasitic series resistance.

For device performance comparison see: http://www.clarycon.com/transistor_perfo.html

“Femto-Second CMOS Technology with High-k Offset Spacer and SiN Gate Dielectric with Oxygen-enriched Interface”

R. Tsuchiya, K. Ohnishi, M. Horiuchi, S. Tsujikawa, Y. Shimamoto, N. Inada, J. Yugami, F. Ootsuka, T. Onai / Hitachi
2002 Symposium On VLSI Technology, Digest of Technical Papers, p. 150

A 40 nm CMOS transistor for the 70 nm node is presented. The leakage current is suppressed by a high-k offset spacer (EOS: high-epsilon offset spacer). The EOS material is SiN. It reduces the external resistance just outside the gate by formation of an inversion layer to maintain a high drive current (0.68 and 0.30 mA/μm for N- and P-MOSFET respectively). The gate delay is very short at 280 fs for an NMOS with 19 nm gate lengths. Other techniques used: SiN gate with oxygen enriched interface, phase shift masks, **resist trimming** and spike annealing.

For device performance comparison see: http://www.clarycon.com/transistor_perfo.html

"Life is CMOS: Why Chase the Life After ?"

G. Sery, S. Borkar, V. De / Intel
Proceedings DAC 2002, p. 78

This paper discusses potential solutions to CMOS technology scaling approaching 10 nm. The key bottlenecks are related to reducing device parasitics (source/drain resistances and gate overlap capacitances). Excessive subthreshold and gate oxide leakage, as well as the overall energy efficiency. Depleted substrate transistors (DST) are discussed. The main challenge for DST's is the control of the silicon thickness because the threshold voltage is quite sensitive to the film thickness. This problem can be alleviated by migrating to metal gate electrodes where the work function influences V_t . Two different metals may be needed for NMOS and PMOS. High k dielectrics are discussed as a solution for the gate oxide leakage problem. The scaling of the gate dielectric thickness is limited by the poly depletion and separation of inversion layer charge from the oxide-silicon interface at high vertical fields due to quantum-mechanical effects. Each of these effects adds 5 Å to the EOT at the highest gate voltage. Increasing the poly doping beyond solubility limit would be desirable. The solution will probably involve metal gates. Design and architecture related techniques are discussed as solutions for leakage control and performance enhancements.

"Vertically Integrated SOI Circuits for Low-Power and High-Performance Applications"

L. Wei, R. Zhang, K. Roy, Z. Chen, D.B. Janes
IEEE Transactions on VLSI Systems, vol. 10. No. 3, 2002, p. 351

This paper demonstrates that the vertical integration offers a path to better circuit performance and power dissipation due to improved device characteristics and reduced interconnect complexity and delay. Structures of vertically integrated double gate (DG) and silicon-on-insulator (SOI) devices and circuits are presented.