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Taking SOI Substrates and Low-k Dielectrics into High-Volume Microprocessor Production

D. Greenlaw, G. Burbach, T. Feudel, F. Feustel, K. Frohberg, F. Graetsch, G. Grasshoff, C. Hartig, T. Heller, K. Hempel, M. Horstmann, P. Huebler, R. Kirsch, S. Kruegel, E. Langer, A. Pawlowitsch, H. Ruelke, H. Schuehrer, R. Stephan, A. Wei, T. Werner, K. Wieczorek, and M. Raab

This paper by Advanced Micro Devices describes the challenges of transferring AMD's 90 nm node into mass production. The technology was developed for the 9-metal AMD Opteron^{TM} and Athlon^{TM}64 microprocessor lines and has the following features: SOI substrate, STI with LPCVD fill, two different gate oxide thicknesses, triple spacers, $CoSi_x$, W plugs, CVD low-k dielectric (k_{eff}<3), Ta barriers. The paper describes the following challenge and solutions to them: large defects of the SOI substrates, bending of the Si islands after STI fill, divots at the surface of the fill oxide, poor contrast for the inline CD measurements on SOI material, accuracy and repeatability of the measurements of the thin gate oxides, profile distortion for the gate etch, floating body effect for the SOI transistors, amorphizing dose/energy and RTA thermal cycle must be retuned at each new Si thickness for the SOI structures, defects associated with the processing of the low-k films, and the reduced mechanical stability of the low-k films during CMP processing.

Low voltage, scalable nanocrystal FLASH memory fabricated by templated self assembly

K. W. Guarini, C. T. Black, Y. Zhang, I. V. Babich, E. M. Sikorski, and L. M. Gignac

A new method for building nanocrystal flash memory devices is introduced by the IBM Semiconductor Research and Development Center. The Si nanocrystals are defined using diblock copolymer thin film self assembly. A diluted polymer solution is spin coated and annealed to promote phase separation into nanometer-scale polymer domains. The diblock copolymer is composed of polystyrene (PS) and poly(methyl methacrylate) (PMMA), whose molecular weight ratio produces hexagonally-closepacked PMMA cylinders in the PS matrix. The PMMA is removed with an organic solvent, leaving a porous PS film, which is used as a sacrificial layer to define nanocrystals at sub-lithographic dimensions. Devices made using this technique show low voltage memory operation with good retention and endurance properties.

High Performance CMOS Fabricated on Hybrid Substrate With Different Crystal Orientations

M. Yang, M. Ieong, L. Shi, K. Chan, V. Chan, A. Chou, E. Gusev, K. Jenkins, D. Boyd, Y. Ninomiya, D. Pendleton, Y. Surpris, D. Heenan, J. Ott, K. Guarini, C. D'Emic, M. Cobb, P. Mooney, B. To, N. Rovedo, J. Benedict, R. Mo and H. Ng

IBM Semiconductor Research and Development Center and IBM Microelectronic Division present a technique to utilize different crystal orientations for pFET (110 oriented surface) and for nFET (100 oriented surface) to increase the mobility of the holes and electrons, respectively. Expitaxial re-growth from the substrate underneath the Box is used to create the second orientation at the surface. CMOS devices with substantial enhancement of pFET drive currents have been demonstrated at L_{poly}=80nm and with physical gate oxide thickness of 1.2 nm.

High Performance CMOS Devices on SOI for 90 nm Technology Enhanced by RSD (Raised Source/Drain) and Thermal Cycle/Spacer Engineering

H. Park, W. Rausch, H. Utomo, K. Matsumoto1, H. Nii, S. Kawanaka, P. Fisher, S-H. Oh, J. Snare, W. Clark, A.C. Mocuta, J. Holt, R. Mo, T. Sato, D. Mocuta, B.H. Lee, O. Dokumaci, P. O'Neil, D. Brown3, J. Suenaga1, Y. Li, L. Brown3, J. Nakos, K. Hathorn, P. Ronsheim, H. Kimura, B. Doris, G. Sudo, K. Scheer, S. Mittl, T. Wagner, T. Umebayashi, M. Tsukamoto, Y. Kohyama, J. Cheek, I. Yang, H. Kuroda, Y. Toyoshima, J. Pellerin, D. Schepis, Y. Li, P. Agnello, and J. Welser

IBM, AMD, Toshiba, and Sony present a 90 nm device with partially depleted SOI with 40 nm gate length, raised source/drain, disposable spacer, final spacer for S/D doping and silicide proximity, and NiSi.

Fabrication and Mobility Characteristics of Ultra-thin Strained Si Directly on Insulator (SSDOI) MOSFETs

K. Rim, K. Chan, L. Shi, D. Boyd, J. Ott, N. Klymko, F. Cardone, L. Tai, S. Koester, M. Cobb, D. Canaperi, B. To, E. Duch, I. Babich, R. Carruthers, P. Saunders, G. Walker, Y. Zhang, M. Steen, M. Ieong

IBM reports on strained MOSFETs which are built directly on insulator structures with no SiGe layer present under the strained Si channel. Without the relaxed SiGe layer present as the lattice template, it is necessary that the insulator layer supports the strain state in the Si layer. SSDOI offers the possibility to scale to Si body and to form fully depleted devices on SOI (FDSOI).

High Speed 45nm Gate Length CMOSFETs Integrated Into a 90nm Bulk Technology Incorporating Strain Engineering

Victor Chan, Rajesh Rengarajan, Nivo Rovedo, Wei Jin, Terence Hook, Phung Nguyen, Jia Chen, Ed Nowak, Xiang-Dong Chen, Dallas Lea, Ashima Chakravarti, Victor Ku, Sam Yang, An Steegen, Christopher Baiocco, Padraic Shafer, Hung Ng, Shih-Fen Huang, Clement Wann

IBM presents a 90 nm logic bulk foundry technology with 45 nm gate length devices incorporating strain engineering utilizing strain from the shallow trench isolation and the contact etch stop layer. Technology features include shallow abrupt source/drain extensions, halo implants, deep source/drain implants and spike activation anneal. Spacer formation and the subsequent thermal cycle were optimized to reduce dopant transient enhanced diffusion (TED) and improve the junction abruptness. Super-halo dopants are confined to the gate edges and the doping profile is very abrupt. Cobalt silicide is formed on the poly and source/drain regions.
For performance comparison see: http://www.clarycon.com/transistor_perfo.html

Device Design Considerations for Ultra-Thin SOI MOSFETs

B. Doris, M. Ieong, H. Zhu, Y. Zhang, M. Steen, W. Natzle, S. Callegari, V. Narayanan, J. Cai, S.H. Ku, P. Jamison, Y. Li, Z. Ren, V. Ku, D. Boyd, T. Kanarsky, C. D'Emic, M. Newport, D. Dobuzinsky, S. Deshpande, J. Petrus, R. Jammy, and W. Haensch

IBM presents an ultra-thin SOI (UTSOI) device as an attractive choice for sub-10nm gate-length scaling. In this work the major issues for UTSOI are addressed. External resistance is minimized by using the Raised EXtension (REX) process flow, which features an offset spacer to minimize the region of UTSOI outside the channel. The REX process scheme is used to demonstrate improved pFET performance and also to demonstrate the first planar single gate nFET with 8nm gate length. High temperature mobility measurements show that the channel thickness can be scaled further than previously predicted. The pFET with L_{gate}=8nm exhibits a sub-threshold swing of 80mV/decade at V_d=-1.2V. The output characteristics show that a drain current of 320µA/µm is achieved at V_{dd}=-1.5V. Gate delay (CV/I) for the pFET with sub-10nm gate-length using the REX process is 0.61ps. In addition, UTSOI devices with tungsten gates and HfO_2 gate dielectrics having appropriate threshold voltages are presented.
For performance comparison see: http://www.clarycon.com/transistor_perfo.html

Performance comparison of sub 1 nm sputtered TiN/HfO2 nMOS and pMOSFETs

W. Tsai, L.-Å Ragnarsson, L. Pantisano, P.J. Chen, B. Onsia, T. Schram, E. Cartier, A. Kerber, E. Young, M. Caymax ,S. De Gendt, M. Heyns

This joint paper by Intel, IMEC, Texas Instruments, IBM, Infineon, and Philips investigates ALD HfO_2 high k dielectrics in conjunction with PVD sputtered gate electrodes. The best performance was obtained with 30 cycles of HfO2 resulting in an EOT of 8.2 Å for the nFET and 7.6 Å for the pFET. The thickness of the chemical oxide interface was controlled by modulating the ozone concentration in DI water with a re-circulating bath to deliver a near-monolayer SiO_x template for high-k deposition. Gate leakage reduction up to three orders of magnitude was achieved with a flatband voltage close to ideal value of -0.27 V and 0.60 V for nMOS and pMOS, respectively. The hole mobility remained constant down to an EOT of 8 Å.

A 90nm High Volume Manufacturing Logic Technology Featuring Novel 45nm Gate Length Strained Silicon CMOS Transistors

T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, B. McIntyre, K. Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zawadzki, S. Thompson, M. Bohr

This paper by Intel created a lot of excitement in the media even before IEDM 2003. It reports on a strained PMOS transistor structure that features an epitaxially grown strained SiGe film

embedded in the source drain regions creating an uniaxial compressive strain in the channel region. One unique feature of this NMOS structure is the integration of a post salicide “highly-tensile” silicon nitride capping layer. The stress from this capping layer is uniaxially transferred to the NMOS channel through the source-drain regions to create tensile strain in NMOS channel. Dramatic performance enhancement relative to unstrained devices are reported. The transistors have gate length of 45 nm and 50 nm for NMOS and PMOS respectively, 1.2 nm physical gate oxide and Ni salicide. Drive currents of 700 µA/µm (high V_T) and 800 µA/µm (low V_T) at 1.2 V are demonstrated. NMOS devices exercise a highly tensile silicon nitride capping layer to induce tensile strain in the NMOS channel region. High NMOS drive currents of 1.26 mA/µm (high V_T) and 1.45 mA/µm (low V_T) at 1.2V are reported.
For performance comparison see: http://www.clarycon.com/transistor_perfo.html

High Mobility Si/SiGe Strained Channel MOS Transistors with HfO_2/TiN Gate Stack
S. Datta, G. Dewey, M. Doczy, B.S. Doyle, B. Jin, J. Kavalieros, R. Kotlyar, M. Metz, N. Zelick and R. Chau
Intel presents an integration scheme with strained Si channel on relaxed Ge_xSi_{1-x} (Ge=10%) virtual substrate, HfO_2 gate dielectric directly on strained Si, and TiN metal gate. For the NMOS transistors, a 35% higher mobility than the unstrained Si control with HfO_2/TiN gate is demonstrated.
For performance comparison see: http://www.clarycon.com/transistor_perfo.html

Performance Improvement of MOSFET with HfO_2-Al_2O_3 Laminate Gate Dielectric and CVD-TaN Metal Gate Deposited by TAIMATA
Seong Geon Park, You Kyoung Lee, Sang Bom Kang, Hyung Suk Jung, Seok Joo Doh, Jong-Ho Lee, Jae Ho Choi, Gyeong Hoon Kim, Gil Heyun Choi, U In Chung, Joo Tae Moon
SAMSUNG presents a paper on MOSFET’s with an integrated HfO_2-Al_2O_3 laminate gate dielectric with CVD-TaN metal gate deposited by TAIMATA (tertiaryamylimidotris dimethylamidotantalum). Substantially improved current derivabilities of 839 µA/µm (I_{off} = 60 nA/µm) and 468 µA/µm (I_{off} = 7pA/µm) for n/pMOSFETs were obtained. In addition, excellent leakage current with F-N tunneling behavior and good subthreshold slopes were observed.
For performance comparison see: http://www.clarycon.com/transistor_perfo.html

Static Noise Margin of the Full DG-CMOS SRAM Cell Using Bulk FinFETs (Omega MOSFETs)
T. Park, H. J. Cho, J. D. Choe, S. Y. Han, S.-M. Jung, J. H. Jeong, B. Y. Nam, O. I. Kwon, J. N. Han, H. S. Kang, M. C. Chae, G. S. Yeo, S. W. Lee, D. Y. Lee, D. Park, K. Kim, E. Yoon, J. H. Lee
SAMSUNG claims the first fully integrated bulk FinFET SRAM cell in collaboration with the Seoul National University (the first SOI FinFET SRAM cell was announced by IBM at the 2002 IEDM). Static noise margin of 280 mV was obtained at V_{CC} of 1.2 V.

Fully Working 1.25µm2 6T-SRAM Cell with 45nm Gate Length Triple Gate Transistors
Jeong-Hwan Yang, You-Seung Jin, Hyae-Ryoung Lee, Kyoung-Seok Rha, Jung-A Choi, Su-Kon Bae, Shigenobu Maeda, Young-Wug Kim, Kwang-Pyuk Suh
SAMSUNG reports the first experimental demonstration of a fully working Triple Gate SRAM cell with the smallest cell size ever reported. The transistor characteristics show excellent short channel effect control down to 35 nm gate length.
For performance comparison see: http://www.clarycon.com/transistor_perfo.html

Highly Performant Double Gate MOSFET realized with SON process
S.Harrison, P.Coronel, F.Leverd, R.Cerutti, R.Palla, D.Delille, S.Borel, S.Jullian, R.Pantel, S.Descombes, D.Dutartre, Y.Morand, MP.Samson, D.Lenoble, A.Talbot, A.Villaret, S.Monfray, P. Mazoyer, J.Bustos, H.Brut, A.Cros, D.Munteanu, J L.Autran,T.Skotnicki
STM and LETI report on a double gate device based on their SON (Silicon On Nothing) process. Drive currents of 1954 µA/µm (I_{off} = 283 nA/µm) and 1333 µA/µm ($_{Ioff}$ = 1 nA/µm) are obtained at 1.2V with T_{ox} = 20A and L_{gate} = 70nm. DIBL is measured below 60mV for gates as short as 40nm.
For performance comparison see: http://www.clarycon.com/transistor_perfo.html

Scalability of Strained Silicon CMOSFET and High Drive Current Enhancement in the 40nm Gate Length Technology

T. Sanuki, A. Oishi, Y. Morimasa, S. Aota, T. Kinoshita, R. Hasumi, Y. Takegawa, K. Isobe, H. Yoshimura, M. Iwai, K. Sunouchi and T. Noguchi

Toshiba addresses the problem that drive current enhancement of strained PMOSFET usually disappears as the device is scaled down due to the stress induced by Shallow Trench Isolation. As the devices get smaller, the hole mobility is expected to degrade in strained Si since the STI-induced stress reduces and eventually compensates strain created by the Si/SiGe structure.

A 65nm Node Strained SOI Technology with Slim Spacer

Fu-Liang Yang, Chien-Chao Huang, Hou-Yu Chen, Jhon-Jhy Liaw, Tang-Xuan Chung, Hung-Wei Chen, Chang-Yun Chang, Cheng-Chuan Huang, Kuang-Hsin Chen, Di-Hong Lee, Hsun-Chih Tsao, Cheng-Kuo Wen, Shui-Ming Cheng, Yi-Ming Sheu, Ke-Wei Su, Chi-Chun Chen, Tze-Liang Lee, Shih-Chang Chen, Chih-Jian Chen, Cheng-Hung Chang, Jhi-Cheng Lu, Weng Chang, Chuan-Ping Hou, Ying-Ho Chen, Kuei-Shun Chen, Ming Lu, Li-Wei Kung, Yu-Jun Chou, Fu-Jye Liang, Jan-Wen You, King-Chang Shu, Bin-Chang Chang, Jaw-Jung Shin, Chun-Kuang Chen, Tsai-Sheng Gau, Bor-Wen Chan, Yi-Chun Huang, Han-Jan Tao, Jyh-Huei Chen, Yung-Shun Chen, Yee-Chia Yeo, Samuel K-H Fung, Carlos H. Diaz, Chii-Ming M. Wu, Burn J. Lin, Mong Song Liang, Jack Y.-C. Sun, Chenming Hu

TSMC reports a 65 nm strained SOI technology with aggressively scaled slim spacer of 30 nm width for transistors with 40 nm gate length. The advantages of this design are an enhanced performance due to significantly reduced R_{SD} , increased strain effects in the transistor channel, and a denser circuit layout. Slim spacer devices were used to built 6T SRAM cells which also included FinFET devices. Special super-halo and light body doping implants were designed to achieve fully depleted (FD) and partially-depleted (PD) SOI devices at different gate lengths. TSMC calls this technology hybrid FinFET/FD/PDSOI (FIP-SOI).
For performance comparison see: http://www.clarycon.com/transistor_perfo.html

Process-Strained Si (PSS) CMOS Technology Featuring 3D Strain Engineering

C.-H. Ge, C.-C. Lin, C.-H. Ko, C.-C. Huang, Y.-C. Huang, B.-W. Chan, B.-C. Perng, C.-C. Sheu, P.-Y. Tsai, L.-G. Yao, C.-L. Wu, T.-L. Lee, C.-J. Chen, C.-T. Wang, S.-C. Lin, Y.-C. Yeo, C. Hu

This paper by TSMC investigates the use of process induced stress to inprove the performance of NMOS and PMOS devices simultaneously. The stress can be introduced during trench isolation, silicide, and cap layer formation. According to TSMC, this low-cost technology is highly manufacturable, is compatible with conventional CMOS processes and is suitable for high-performance CMOS applications.

Characterization and Comparison of the Charge Trapping in HfSiON and HfO2 Gate Dielectrics

A. Shanware, M. R. Visokay, J. J. Chambers, A. L. P. Rotondaro, J. McPherson, L. Colombo, G. A. Brown, C. H. Lee, Y. Kim, M. Gardner, R. W. Murto

Texas Instruments and SEMATECH report on the electrical stability of NMOS devices using HfO_2 and HfSiON gate dielectrics using both DC and pulsed techniques. This study shows that HfSiON gate dielectric is more stable than HfO_2. Constant voltage stress measurements of HfO_2 and HfSiON films also show that the threshold voltage shift in HfO_2 films is as much as 10 times higher than that of HfSiON. The authors attribute the stability in HfSiON gate dielectric as being due to lack of crystallization resulting in a significantly lower number traps and a much lower (10x) lower capture cross section compared to traps in the HfO_2.