Literature Digest
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Plasma Physics

"Radical dynamics in unstable CF_4 inductive discharges"
P. Chabert, H. Abada, J.-P. Booth, M. A. Lieberman
J. Appl. Phys. 94 (2003) 76

This paper describes studies on plasma instabilities in a pure CF_4 plasma exited at 13.56 MHz by a planar spiral coil through an alumina window. The amount of capacitive coupling was influenced by whether or not the coil was terminated by a 400 pF capacitor. With the 400 kHz termination, the fluctuation frequencies were in the range of several hundred Hz which is similar to previous studies with quartz windows (reduced capacitive coupling compared to alumina windows). The oscillation frequencies are power, pressure and gas flow dependent and the instability period is always smaller than the gas residence time. For the non-terminated coil, the oscillation frequencies are much lower, between 0.5 and 15 Hz. The instability periods are much longer than the residence time of the molecules in the reactor. In addition, the instability frequencies were not reproducible for the coil without 400 pF termination. For these two reasons the authors believe that with this electrical configuration, slow and erratic mechanisms are involved. The authors hypothesize that polymer deposition on the reactor walls may have a significant effect on the plasma chemistry and consequently on its stability. Also, particle sputtering of the alumina window could lead to the formation of negative ions which could remove electrons until the plasma is cannot be sustained in the inductive mode. The CF and CF_2 radical dynamics for the 400 pF terminated coil were investigated by means of laser induced fluorescence (LIF) and plasma induced emission (PIE). The radical densities for CF and CF_2 vary significantly during the plasma instabilities. Chemical reactions (either in the gas phase or at the wall) seem to be mainly responsible for the radical density fluctuations, at least in low-pressure discharges (1 mTorr). Gas heating effects, observed previously in the inductive mode, probably make some contribution to the radical dynamics at higher pressure, but do not explain the major part of the observed time variations. A global model originally developed for Ar/SF_6 mixtures was adapted to the given system system. As in SF_6 , the model predicts frequencies and densities that are too small but the general trends are respected; for example, the model predicts that the instability frequency in CF_4 is about 30 times smaller than in SF_6, in good agreement with experimental observations.

These findings show the importance of the reactor design (thickness and material of the dielectric window, reactor size, chamber wall materials) as well as the process chemistry (flow of electronegative gases, polymerization rate of these gases) when inductively coupled reactors are being used for advanced etches which increasingly require extreme levels of repeatability and reproducibility.

Plasma Etching: Chamber Wall Effects

"Effects of chamber wall conditioning on Cl concentration and Si etch rate uniformity in plasma etching reactors"
T.-W. Kim, E.-S. Aydil
J. Electrochem. Soc. 150 (2003) G148

The subject of chamber wall effects in inductively coupled plasma etch reactors is one of the intensively studied aspects of plasma etching due to the relevance for advanced device manufacturing. For other papers on this subject please see Clarycon Literature Digests vol. 4 and 8. This paper focuses on the spatial Cl radical distribution as a function of chamber wall coverage

with silicon oxychloride and the resulting change in the etch rate disribution across the wafer. As the reactor walls are coated with silicon oxychloride, the etch rate distribution changes from center-fast to edge fast due to a reduced depletion of chlorine radical at the chamber wall.

High k Dielectrics

"Electronic structure analysis of Zr silicate and Hf silicate films by using spatially resolved valence electron energy-loss spectroscopy"
N. Ikarashi, K. Manabe
J. Appl. Phys. 94 (2003) 480

The authors show that the electronic structure of Zr silicate can be reproduced by a superposition of the electronic structures of ZrO_2 and SiO_2 and that of Hf silicate by a superposition of the electronic structures of HfO_2 and SiO_2. This indicates that, in these silicates, the lowest conduction band states are composed mostly of *d* states of Zr or Hf, and the valence band states mostly of O 2*p* states. The d states of Zr and Hf play therefore an important role in determining the gate leakage current for these materials in MOSFET devices.

"Characterization of La_2O_3 and Yb_2O_3 thin films for high-k gate insulator application"
S. Ohmi, C. Kobayashi, I. Kashiwagi, C. Ohshima, H. Ishiwara, H. Iwai
J. Electrochem. Soc. 150 (2003) F134

This work was conducted by the Tokyo Institute of Technology and supported by the semiconductor consortium STARC. The motivation for the study was based on recent reprts on rare earth oxides such as amorphous La_2O_3 (A. Chin et al., Proceedings of the Symposium on VLSI Technology, 16 (2000)), epitaxial Pr_2O_3 (H.J. Osten et al., Tech. Dig. – Int. Electron. Deveices Meet. (2000) 653), Nd_2O_3, Sm_2O_3, Gd_2O_3, Dy_2O_3 and others (J.A. Gupta et al., Appl. Phys. Lett. 78 (2001) 1718 and S. Jeon et al., Tech. Dig. – Int. Electron. Deveices Meet. (2001) 471). The two materials in this study were chosen because of their large difference in lattice energy: La_2O_3 has the lowest lattice energy of all rare earth oxides with –12.687 KJ/mol and Yb_2O_3 the second highest with –13.814 KJ/mol. La_2O_3 has the largest band gap of 5.5 eV while the band gap of Yb_2O_3 is smaller (4.9 eV). La_2O_3 showed excellent electrical properties, such as small capacitance equivalent thickness and low leakage current density ($5E^{-4}$ A/cm^2 for a CET of 0.88 nm and $1.7E^{-8}$ A/cm^2 for a CET of 1.26 nm at 1V) with smooth film surface and interface after rapid thermal annealing at 400 to 600 ºC. In contrast, Yb_2O_3 was easily roughened after rapid thermal annealing even at 400 ºC and showed higher leakage currents ($1.3E^{-2}$ A/cm^2 for a CET of 1.3 nm at 1V). The authors conclude that the lattice energy is one of the important properties in choosing high k gate dielectric materials.

"MOSFET gate leakage modeling and selection guide for alternative gate dielectrics based on leakage considerations"
Y.-C. Yeo, T.-J. King, C. Hu
IEEE Trans. Electron Devices 50 (2003) 1027

This paper provides guidelines for the selection of gate dielectrics to satisfy the off-state leakage current as given by the ITRS roadmap for future high performance and low-power technologies. They key motivation for this investigation is the search of suitable dielectric candidates involves significant research efforts, which require that the selected material can be used for several device generations. The scaling limits of various gate dielectrics is explored based on their direct-tunneling characteristics and the ITRS gate-leakage requirements (which are subjected to change). An important observation is that high k dielectrics that are less leaky at a given $t_{ox,equ.}$ also have a larger slope in the leakage current vs. oxide thickness plot ($\log(J_G) - t_{ox,equ.}$). This can be explained by the fact that the change in the physical thickness for a given change in $t_{ox,equ.}$ is larger for the material with the higher permittivity. This means that the leakage reduction factor

resulting from the replacement of silicon oxide with high k materials becomes smaller as $t_{ox,equ.}$ is scaled down. This property has dramatic consequences for the scalability of high k gate dielectrics. The authors conclude that for high-performance and low-operating-power logic applications, Si_3N_4 or SiO_xN_y will be usable through 2016. A high-k gate dielectric has to be introduced by 2007 for low standby-power technologies. The analysis suggests looking beyond HfO_2 and Al_2O_3, e.g., La_2O_3, for long-term utilization beyond 2010 in the most aggressive gate dielectric scaling scenario.

Devices

"Physical and electrical characteristics of HfN gate electrode for advanced MOS devices"
H.Y. Yu, H.F. Lim, J.H. Chen, M.F. Li, C. Zhu, C.H. Tung, A.Y. Du, W.D. Wang, D.Z. Chi, D.-L. Kwong
IEEE Electron Device Lett. 24 (2003) 230

This paper investigates the physical and electrical properties of PVD HfN as a gate electrode material. HfN possesses midgap workfunction in (TaN)/HfN/SiO_2/Si MOS structures. HfN shows excellent thermal stability (to up to 1000 ºC) on silicon oxide. The authors conclude that HfN is an ideal candidate for fully depleted SOI and/or symmetric double gate MOS device applications.

"Electrical charqacterization of germaniu p-channel MOSFET's"
H. Shang, H. Okorn-Schmidt, J. Ott, P. Kozlowski, S. Steen, E.C. Jones, H.-S. P. Wong, W. Hanesch
IEEE Electron Device Lett. 24 (2003) 242

Compared to silicon, germanium offers a 2 times higher mobility for electrons and a four times higher mobility for holes. In order to use this effect in surface channel devices, one has to come up with a solution for the gate dielectric since Ge oxides are not stable. This paper reports on a Ge PMOSFET device with a 6 nm GeON and a 3 nm LTO gate dielectric and an Al gate electrode. The device has an excellent subthreshold slope of 82 mV/dec. The hole mobility is enhanced by about 40 % compared to the Si control.

"RF characterization of metal T-gate structure in fully-depleted SOI CMOS technology"
S. Lam, H. Wan, P. Su, P.W. Wyatt, C.L. Chen, A.M. Niknejad, C. Hu, P.K. Ko, M. Chan
IEEE Electron Device Lett. 24 (2003) 251

This paper investigates a structure recently proposed by C.L. Chen et al. (IEEE Electron. Device Lett. 23 (2002) 52). As expected, the metal T-gate structure gives a significant reduction in gate resistance. Because of this, the metal T-gate FD-SOI MOSFET achieves a higher f_{max} of 67 GHz as compared with 12.5 GHz in the silicided polysilicon gate counterpart. However, the metal T-gate FD-SOI MOSFET has a lower f_t of 35 Ghz as compared with 44 GHz for the self-aligned polysilicon gate. The extracted parameters reveal that the T-gate structure results in an extra 40% and 80% increase in the parasitic capacitances and respectively. The increase of the gate capacitances (C_{gs} and C_{gd}) comprises generally two components, namely the overlap capacitance C_{ovm}, of the metal-gate-to-source–drain, and the lateral flux capacitance of the gate metal strip with the neighboring source–drain interconnects. Possible ways to optimize the performance of the device include the use of low-k dielectric structures as sidewall spacers to reduce the parasitic gate capacitances, the reduction of the width of the metal T-shaped head, and raised source / drains to reduce the series resistance.

"High performance fully-depleted tri-gate CMOS transistors"
B.S. Doyle, S. Datta, M. Doscy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, A. Murthy, R. Rios, R. Chau
IEEE Electron Device Lett. 24 (2003) 263

Intel reports on a 60 nm fully depleted tri-gate CMOS transistors on SOI. In contrast to a FinFET transistor, which has two gates on the side of the Fin, the tri-gate transistor has an additional gate on the top. No halo implants were used for V_t adjustment, nor were any angled implants necessary to fabricate the devices. The physical gate oxide of the polysilicon gate was 15Å. Raised source / drains were used to reduce parasitic resistances. The transistors have a physical gate length L_g of 60 nm, a height T_{Si} of 36 nm, and a width W_{Si} of 55 nm. The width of the transistor Z equals ($2*T_{Si} + W_{Si}$). The transistors show near-ideal subthreshold gradient and excellent DIBL behavior, and have drive current characteristics greater than any non-planar devices reported so far, for correctly-targeted threshold voltages. The tri-gate devices also demonstrate full depletion at silicon body dimensions approximately 1.5–2 times greater than either single gate SOI or non-planar double-gate SOI for similar gate lengths, indicating that these devices are easier to fabricate using the conventional fabrication tools. Comparing tri-gate transistors to conventional bulk CMOS device at the same technology node, these non-planar devices are found to be competitive with similarly-sized bulk CMOS transistors. Furthermore, three–dimensional (3-D) simulations of tri-gate transistors with transistor gate lengths down to 30 nm show that the 30 nm tri-gate device remains fully depleted, with near-ideal subthreshold swing and excellent short channel characteristics, suggesting that the tri-gate transistor could pose a viable alternative to bulk transistors in the near future.

For device performance comparison see: http://www.clarycon.com/transistor_perfor.html

"Theory of electron-mobility degradation caused by roughness with long correlation length in strained-silicon devices"
I. Kitagawa, T. Maruizumi, N. Sugii
J. Appl. Phys. 94 (2003) 465

To study influence of surface roughness of a strained-Si/SiGe heterostructure on electron mobility, electron-transport properties were investigated with the ensemble Monte Carlo method. In the simulation electrons were treated as three dimensional-electron-gas models. Ionized impurity scattering, intra-valley acoustic-phonon scattering, and non polarized inter-valley optical phonon scattering were considered as scattering mechanisms. To consider the influence of roughness with a long correlation length (>100 nm), an electron-motion-deviation model, in which the direction of momentum of electrons was deflected according to the roughness in the channel, was devised. It was found that roughness degraded drift velocity and electron mobility. Electron mobility decreases with decreasing correlation length of roughness ($100<\lambda<800$ nm). It was also found that mobility strongly depends on the amplitude of roughness with a correlation length in the range 100–500 nm. The results show that the decrease in amplitude of roughness is the appropriate way to improve electron mobility in strained SiGe devices. The roughness is originated in the formation process of the SiGe layers. During heteroepitaxial growth of a $Si_{1-x}Ge_x$ layer on a silicon substrate beyond the critical thickness, misfit dislocations are formed and propagate as strain relaxation of the $Si_{1-x}Ge_x$ layer proceeds. This dislocation propagation increases the surface roughness. Therefore, it is imperative to reduce the defect concentration during the manufacturing of strained SiGe devices.

"A view of nanoscale electronic devices"
H. Mokoc, Y. Taur
J. Korean Phys. Soc. 42 (2003) S555

This excellent review paper describes conventional MOS scaling and makes predictions about future technologies beyond conventional CMOS technology: high k dielectrics, double-gate MOSFET's, single electron transistors, and carbon nanotubes. The authors state that the dramatic progress in VLSI technology has mainly been accomplished by constant field scaling. The scaling rules are given in the following table:

	MOSFET Device and Circuit Parameters	Multiplicative Factor
Scaling assumption	Device dimensions (tox, L, W, Xj)	1/k
	Doping concentration (Na, Nd)	k
	Voltage (V)	1/k
Derived scaling behavior of device parameters	Electrical field (E)	1
	Carrier velocity (v)	1
	Depletion layer width Wd)	1/k
	Capacitance (C)	1/k
	Inversion layer charge density (Qi)	1
	Drift current (I)	1/k
	Channel resistance (Rch)	1
Derived scaling behavior of circuit parameters	Circuit delay time (τ)	1/k
	Power dissipation per circuit (P)	$1/k^2$
	Power-delay product per circuit ($P*\tau$)	$1/k^3$
	Circuit density	k^2
	Power density	1

The key assumption for these scaling rules is that the threshold voltage also scales down by k. However, the diffusion current does not scale down the same way as the drift current. This has the consequence that the MOSFET subthreshold currents don't follow the scaling rules which forces the operating voltage not to scale. The challenges in scaling are among others short channel effects, an increasing power dissipation per chip, tunneling and dopant fluctuations. Also, as field effect transistors are scaled down and the device dimensions are becoming comparable to the scattering length, conventional concepts of drift and diffusion will not apply and one must invoke ballistic or quasi ballistic transport. The ultimate scaling limit for double-gate MOSFET's is given with a device length of 10 to 15 nm.

Nanotechnology

"A molecular electronics tool box"
A.M. Rawlett, T.J. Hopson, I. Amlani, R. Zhang, J. Tresek, L.A. Nagahara, R.K. Tsui, H. Goronkin
Nanotechnology 14 (2003) 377

The authors from the Physical Sciences Research Laboratories of Motorola describe an effort to develop a molecular "toolbox" containing organic molecules, carbon nanotubes (CNT's), DNA molecules and nanoparticles. Three methods of electrically testing molecular scale components are presented: Conducting AFM to contact single or small groups of molecules, ac trapping of Au nanoparticles between self assembled monolayer (SAM) covered contacts for rapid electronic measurements, and reduced pressure chemical vapor deposition growth of CNT's. The catalyst for the CNT growth was a mixed salt solution of $Fe(SO_4)_3/(NH_4)_4Mo_7O_{24}/H_2O$ with a molar composition of $Fe:Mo:Al_2O_3$ of 1:17:16 (from A.M. Cassell et al.; J. Phys. Chem. B103 (1999) 6484).